REMARKS

In respons to the Examiner's Office Action of February 28, 2003, and with the papers requesting a One-Month Extension of Time, Applicant is hereby providing his response to Examiner's Office Action.

In regard to missing Figs. 6A and 6B, Applicant is attaching a new set of drawings which include the Figs. 6A and 6B. It was unknown as to why these two figures should be missing, since the mailings are generally checked for inclusion of all documents. However, it is regretted that these two figures were not present when the Examiner received the documents.

Additionally, Applicant is forwarding a new set of drawings which will include all the corrections which Examiner indicated should be taken care of. Thus, in Fig. 2A, the item "29ex" has now been added to the specification to indicate that this represents an expanded epoxy scattering.

In Fig. 2B, the component 39 has now been labeled 39a in accordance with page 10, line 18. Likewise, in Fig. 2B, as indicated by the Examiner, Applicants have now applied a more consistent numbering system so that the elements 29a are comparable to 39a and 49a. Likewise, the terminal pads have been added and indicated as 29b, 29c and then 39b and 39c, and then 49b and 49c. Thus, the numbered items of Fig. 2B should now appear to be more consistent.

Further corrections were made to page 10 to indicate the items 29a, 39a, and 49a. Likewise on page 12 the phrase "test that circuit 30 connect d" has been corrected to read --test sock t 30 conn cted--.

Another correction has be n made to page 18, line 6 where th cited Fig. 5A should actually read --6A--. This shows the step N.

The Examiner has rejected the claims for obviousness under 35 USC 103(a), wherein the Examiner has combined a series of references to *Kondo,* to Japanese Application 10-239373 to *Agawa* in view of the patent 4,739,258 to *Schwartz,* and U.S. Patent 5,844,330 to *Furukawa*. While these references may partially refer to certain facets that might be collaterally related to Applicant's invention with a great stretch of imagination, Applicant, at this point, would traverse the Examiner's reasoning as to the applicability and combinability of these various references.

The *Kondo* reference, patent 4,938,410, involves a "soldering" apparatus of the reflow type. Pre-heating and reflow chambers are provided with heaters for heating printed circuit boards with the chips temporarily mounted thereon with solder pastes. The idea is to remove bubbles generated upon fusion of the solder pastes, and to minimize heat shock to the chips as they are heated. Applicant would contend that this *Kondo* patent for soldering apparatus is not relevant to the methodology and type of operation provided by Applicant. Besides, *Kondo* does not involve a testing program for miniature integrated circuit elements, as does Applicant's. *Kondo* is addressing the problem of soldering components while eliminating solder bubbles.

The *Schwarz* patent involves a method and apparatus for evaluating the reliability of a thin film conductor. Here, the object is to determine the values of activation energy (Q) and the pre-exponent (A) associated with the electro-migration process for int grated circuits on the same semi-conductor wafer.

Schwarz uses high current densities that elevat temperatur s. *Schwarz* provides for lectrically stressing the thin film conductor by applying a constant or uniform current to it. At the same time, a ramp current is provided to the resistive heating element so that the stressed thin-film conductor is heated at a rate that increases linearly with respect to time. Then *Schwarz* measures changes in resistance of the current stressed conductor. After this, the activation energy Q and the pre-exponential factor A are calculated by relating the measured changes in resistance over time to a particular rate expression indicated as:

$$1/R_0.dR/dt=Aexp(-Q/kT)$$

> *Schwarz* is concerned with the problem of electro-migration failure and using devices to measure the kinetic parameters of this phenomenon. He is not concerned with controlled temperature ramps. It is noted that *Schwarz* (col. 6, lines 33-49) uses a programmable temperature controller to provide a programmed temperature ramp in a precise linear increasing rate over a period of time from several minutes up to 100 hours.
>
> This is not a teaching for a "non-destructive" 20 degree Celsius up ramp and down ramp to solve the problem of spotting possible intermittent failures. *Schwarz* goes to the level of current stressing to the point of destruction of the component.

It should be emphasized that while a component appears normally op rable, it will show its intermitt nt erratic and faulty b havior during the temperatur ramping. It is only then

that the intermittent short or open circuitry defect will b observable.

The Patent of *Furakawa*, U.S. Patent 5,844,330 involves the method for effecting the discharge of a capacitor component. A capacitor component is mounted on a printed wiring board by solder to the first and second electrodes between which a capacitance is generated. Then, there is a short-circuiting member to electrically connect the first and second terminals, with the short-circuiting member having a portion to be molten to cut by heating.

> As will be seen in claim 1 of *Furukawa*, there is a vacuum head having an opening, said hollow inside portion communicating to the opening end, said hollow inside portion being given a vacuum to attract the capacitor component by suction: and --- a conductive pad to short-circuit said first and second terminals . . . . etc.
>
> > Applicant would contend that this capacitative shorting device has little to do with any teaching provide by Applicant for the non-destructive testing of miniature integrated circuit components which may have short-circuits or other intermittent failures due to an over-abundance of epoxy contact material. *Furakawa* does not attack the problem of testing to find intermittent defects.

The patent to *Suski,* U.S. Patent 5,419,780 involves an apparatus to remove h at from a semi-conductor device which

involves a thermo- lectric generator to conv rt heat energy to el ctrical en rgy and the thermo-el ctric generator produces an output voltage in response to said heat --- and additionally, there is an airflow generating device electrically connected to the output voltage from said thermo-electric generator to cause the air to flow and the air flow generated device is positioned proximate to the semi-conductor so that air is caused to flow by said air flow generating device to remove heat from the semi-conductor and reduce the temperature of the semi-conductor device.

> The fact that a fan can be used as cooling device is only one minor aspect of Applicant's method and technology for testing integrated circuit components.

The patent number Re.32,625 to *Schwarz* is again quite similar to the previously-mentioned *Schwarz* reference in that it involves a method for determining the kinetic parameters of activation energy and the pre-exponential factor which characterizes electro-migration failure in a thin-film conductor that is subject to high current densities at elevated temperatures.

> It may be helpful to define "electro-migration failure". *Note*: The type of failure called "electro-migration failure" generally involves a movement of atoms in the direction of current flow from a first donor region into a second acceptor region. Electro-migration failure occurs in two separate stages. During the first stage called the " l ctro-migration damage" (EMD), the atoms move out of the donor region under

> r latively well-defin d conditions leaving behind voids in th material. The transported atoms ar deposit d in the acceptor region thereby creating hillocks --- the second stage of electro-migration failure referred to as the "catastrophic failure" process (CFP) stage, is characterized by complex temperature and current density variations that lead to a rapid and complete failure of a device.

This *Schwarz* procedure does not solve the problem of non-destructive testing to find intermittent defects. *Schwarz* operates to destruction of the component.

The *Agawa* reference from the Patent Abstracts of Japan, Publication 10-239373, involves the detection of parts in a printed circuit board which have an abnormal function due to a short-circuit --- this is done by producing an alarm from the resistance value between a power source line and a common line of the printed circuit board when it is reduced less than a fixed threshold value.

> Notice that the resistance involved here is set to trigger a signal when the resistance falls below a certain fixed threshold -- that is, the resistance between the power supply line and the common line.
>
> This method would not flush out "intermittent" defects.

Note, that *Agawa* is merely an individual check for shorts by a "short checker". A hand probe is used in order to check the resistance betw en the power supply

pin and th common pin, such that when this resistance falls b low a certain fixed threshold, th n a signal is given to indicate a defective part.

> Certainly, this individual type of checking does not manage to come close to the functions of Applicant's method and system for testing component intermittency and integrated circuit reliability over a selected temperature range, and to graphically log those results to show certain components as defective or as having intermittent defects.

Applicant has now indicated that there are certain factors and features which provide for unusual sensitivity and efficiency for testing components and integrated circuits in a very short period of time. Applicant has indicated a series of modular test components which all work together to allow this testing to occur accurately, with graphic reports indicating behavior. None of the cited references can come close to accomplishing the tasks that are accomplished by Applicant's method and system. Notice Applicant's Fig. 3A, for example, where the normally non-destructive temperature ramp indicates, by its erratic nature, that there is an intermittent defect. The simple probe of *Agawa* would never reveal this defect. The attached Appendix I will cast some extra light on Applicant's test program.

> The combining of references is <u>improper</u> unless the cited reference states or indicates or implies that a certain oth r type of technology would be suitabl for

combination with it. Som light th reon is cast by the following citations.

In the case of *Monarch Knitting Machinery Corporation v. Sulzer Morat GmbH*, shown at 45 USPQ2d, p.1978, decided March 10, 1998 by the U.S. Court of Appeals, Federal Circuit, the question of combining references to show obviousness was discussed as follows:

> Although "trend" may constitute suggestion or teaching to one of ordinary skill in art to make "minor" changes from prior art in accordance with that trend in order to produce the claimed invention, existence of trend depends on content of prior art and trial court may not proceed to find trend without first determining whether prior art contains suggestion or motivation to combine references to form such trend. (underlines added)

It should be indicated herein that there is no suggestion or reason for motivating someone to take the *Kondo* and *Agawa* references and combine them with *Schwarz* and *Furukawa* referen·es --- especially when none of these references are concerned with non-destructive testing for "intermittent" defects in components being temperature cycled over a non-destructive temperature range.

In the case of the *Gentry Gallery, Inc. v. The Berkline Corporation*, decided January 27, 1998, by the U.S. Court of Appeals, Federal Circuit, as reported at 45 USPQ2d, p.1498:

> Defendant failed to establish that invention of patents for sectional sofa with console between two reclining chairs would have been obvious in view of two prior art references in combination, since m r possibility that

ref r nces could hav b en combin d is insufficient to demonstrat that claimed invention would hav been obvious, in that inv ntion of patent r quires "fixed console" between recliners, which neither reference provided and since even if claimed invention only involved physical insertion of free-standing recliner of first reference into second sectional sofa of second reference, such simplicity alone is not determinative of obviousness. (underlines added)

Again, on the question of combining references and obviousness, there is cited the case of ***WMS Gaming, Incorporated v. International Game Technology***, decided July 20, 1999, by the U.S. Court of Appeals, Federal Circuit, where it was stated:

> Federal District Court did not clearly err in finding that invention of patent for virtual reel slot machine would not have been obvious in light of three prior art references in combination, since, accepting District Court's finding that prior art machines merely simulate physical reels of standard mechanical slot machine, it was not clear error for Court to conclude that those machines do not teach non-uniform mapping of numbers to stop positions on machines' reels in order to decrease odds of winning, as claimed in patent, since there is nothing in those references that indicates motivation to combine their teachings with those of third reference that teaches every aspect of claimed invention except non-uniform mapping of numbers to stop positions, and since infringement plaintiff presented objective evidence of non-obviousness in form of commercial success and long usage. (underlin s added).

None of th cited r f rences have addressed the problem solved by Applicant.

It should be noted that Applicant's combination involves a considerable number of inter-cooperating elements which include the computer-controlled fan power supply, the programmable power supply, the temperature meter, the digital multi-meter, the personal computer, the heat sink, the *Peltier* thermo-electric module, the aluminum temperature transfer block, the device under test, and the test socket.

This provides a unique combination of inter-cooperating elements which cannot be synthesized or inherently re-constituted from the type of references cited by Examiner, and no combination of the references could indicate intermittent defects such as shown in Applicant's Fig. 3A.

Thus, Examiner is exhorted to view Applicant's method and system as a whole in its entirety and then subsequently provide a Notice of Allowance therefor.

Respectfully submitted,

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Certificate of Mailing (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Patti S. Preddy

Date: June 23, 2003

Patti S Preddy

APPENDIX I

PURPOSE OVERVIEW

To detect shorted and/or open components caused by the conductive epoxy used in attaching such components.

These components are connected electrically between the Vcc power bus and ground. Because of the circuit configuration the effect on the total resistance when a component is shorted, the effect will depend on where in the circuit the component is located. In some cases, the total resistance is well below the standard deviation. This can be easily detected with a standard resistance check.

There is a significant number of components, that when shorted, their effect on the total resistance will not bring it outside the standard deviation!

There is also a concern for the potential intermittent shorting of high current components. Their paths are capable of conducting high currents and hence, could cause excessive heat that could ignite the substrate material. The substrate is made of PCB material.

The purpose of this test approach is to detect the last two groups of components.

The proposed test is based on the fact that normal resistors have a linear temperature co-efficient. The resistance caused by an intermittent conductive epoxy is not linear since it has formed the contact surface and the quality of contact. The characteristics of this contact vary with a temperature change and will be erratic and non-linear, indicating a problem area.

These non-linear changes affect the total resistanc of the circuit and can be det cted by plotting th resistance change against a controlled temperature chang .

The proposed test applies a constant current of 1mA to the circuit under between Vcc and ground to measure resistance. To monitor the resistance, we used a digital voltmeter to measure the voltage drop across the circuit to be tested. We used a digital voltmeter with an IEEE interface connected to a PC. The PC was used to collect the data from the voltmeter and to control the temperature ramp. The sampling was selected to be able to detect rapid changes without creating excessive data.

The temperature range of 20 degrees Celsius was selected as not to stress the circuit but rather than to create a temperature change within the normal operating range to monitor the linearity of the circuit or erratic graphics as affected by intermittent conductive epoxy contacts or potential conductive epoxy shorts.